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An Asymmetric Multilevel Converter Topology with a Single Source

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Abstract: This paper concerns with the asymmetric multilevel converter that can produce increased number of output voltage waveforms using a single dc source with reduced number of power electronic components. The role of power electronic switches is very important in designing a multilevel converter because it defines the cost, complexity, and circuit size and installation area. The prime function of multilevel converter is to abolish total harmonic distortion and to incorporate desired ac voltage from several separate dc sources. Each level consists of H-Bridge converter units. High efficiency, high voltage capability, lower switching losses are its prime advantages. A multilevel power converter structure can be introduced as an alternative in medium voltage and high power situations. This structure not only achieves high power ratings but also empower the use of renewable energy sources. It finds its basic application in adjustable speed drives, Static Var Compensator (STATCOM).

Index Terms: Asymmetric; Multilevel Inverter; SVM; Cascaded H-Bridge

1. INTRODUCTION

The researchers started working in the concept of multilevel converter in 1975[1]. The fundamental concept of a multilevel converter is to achieve high power. It uses a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion. The multilevel converters can act as both a converter and an inverter. They can produce large number of output voltage levels with high voltage capability. The multilevel converters have more than two output voltage levels with respect to a reference point. The concept of multilevel converters began with the three level converters. For a medium voltage grid, it is difficult to associate only one power semiconductor switch directly. Thus, a multilevel power converter introduces a substitute in high power and medium voltage situations [2]. A multilevel converter finds several advantages over a conventional two level converter that uses high switching frequencies pulse width modulation (PWM) [3].

i. *Staircase waveform quality*: The converter not only generates output voltage with low distortion but also low dv/dt stress.
ii. *Common-mode (CM) voltage*: The converters produce smaller common mode voltage; hence, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. The common mode voltage can be eliminated using the advanced modulation strategies.
iii. *Input current*: Multilevel converter can tie input current with low distortion
iv. *Switching frequency*: The converters can operate at both principal switching frequency and high switching frequency PWM.

On the basis of configuration, the converters can be divided as symmetric, asymmetric and cascaded form multilevel converter [4]. The symmetric multilevel converter uses dc sources of similar values, while asymmetric multilevel converter uses dc sources of unequal values. The cascaded multilevel converter uses the configuration of either symmetric or asymmetric multilevel converter.

Multilevel converters also have some disadvantages. The greatest of them is the requirement of greater number of semiconductor switches [5]. Lower voltage rated switches can be utilized, but each switch will require a related gate drive circuit. This can increase the overall complexity and cost of the system. In general, there are three types of multilevel converters: 1) Neutral Point Clamped (NPC); converter 2) Flying Capacitor (FC) converter; 3) Cascade H-Bridge (CHB) converter.

The main drawback of NPC converter is the unequal voltage in the midst of series connected capacitors. Moreover, this structure needs large number of clamping diodes for higher levels [6]-[8]. Contrary to this, the FC converter requires large number of storage capacitors for higher output voltage levels and capacitor voltage balancing is difficult. Conventional cascade multilevel converter is the most important amongst the used topologies because it requires least number of components [9]. A cascaded multilevel converter comprises of

H-bridge cells. The major drawback is that it requires large number of isolated dc supplies. This can increase the overall complexity of the system. So, to overcome it, split source capacitors are used [10].

Numerous studies have been made by the researchers for the control on multilevel converter. They can be different on the basis of configuration [11]. For asymmetric multilevel converter, voltage vector approximation technique is applied, which is a type of fundamental frequency control. Whereas for symmetric multilevel converter, both low switching and high switching frequencies are considered. These approaches include space vector modulation, multicarrier PWM strategy, amplitude control and harmonic reduction.

2. PROPOSED 19 LEVEL ASYMMETRIC MULTILEVEL CONVERTER

The block diagram below shows the proposed work of asymmetric multilevel converter.

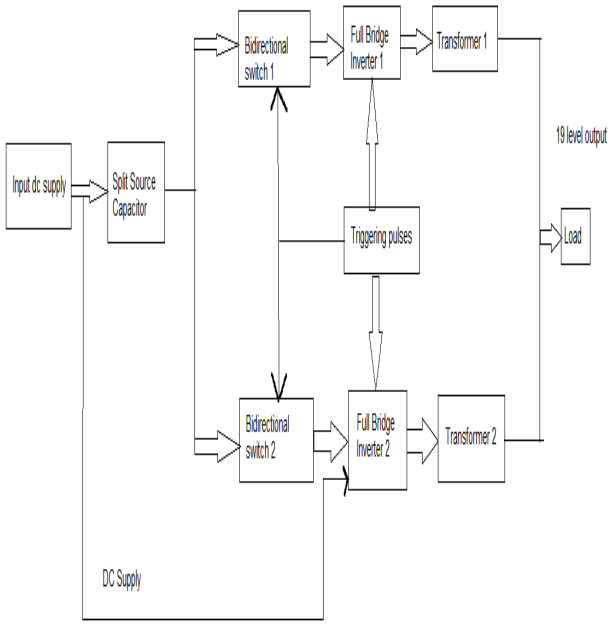

Figure 1. Block Diagram of 19 Level Asymmetric Multilevel Converter

The proposed system of asymmetric multilevel converter consists of a single dc source. The asymmetric multilevel converter provides an optimized number of output voltage levels for the same number of power electronic devices when compared to its symmetric counterpart. It should be noted that a multilevel converter can act both as an inverter and a rectifier. The cascaded H-Bridge topology is used to get the desired number of levels. Each switch is comprised of H-bridge cells. Each block of switches is provided with a triggering pulse. The major disadvantage of cascaded H-bridge cells is that it requires greater number of isolated dc sources in the input side. The greater number of dc sources can increase the complexity of the circuit and cost. To minimize this complexity, split source capacitors are used. The main function of these capacitors is to equally divide the input voltage source amongst the power electronic switches. The methodology used in the multilevel converter is the space vector modulation technique.

3. METHODOLOGY

The space vector PWM technique is an algorithm for control of pulse width modulation. It is commonly used to drive 3 phase ac powered motors at alternating speeds from dc using multiple Class D amplifiers. One active area of development of SVM is in the reduction of total harmonic distortion (THD) created by rapid switching inherent to these algorithms (figure 2).

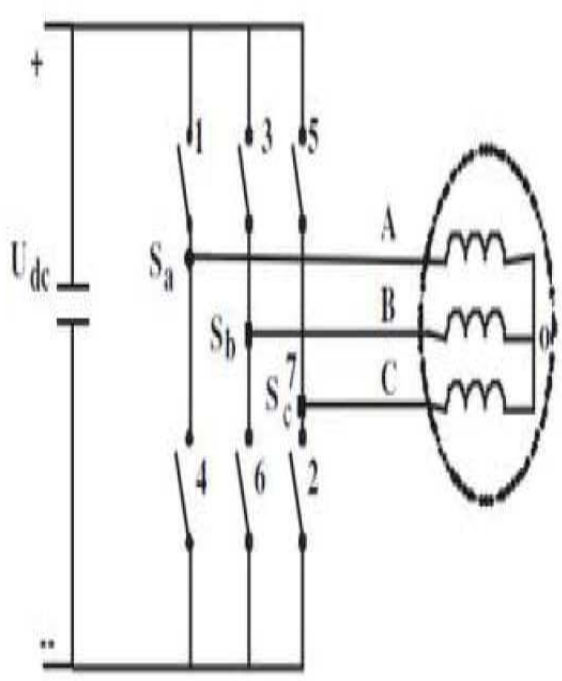

Figure 2. Topology of a basic three phase inverter

An inverter is commonly used in variable speed AC motor drives to yield a variable, three phase, AC output voltage from a constant DC voltage. Basically, amplitude and frequency defines the two characteristics of AC voltage. Thus it is essential to work out a strategy on how to control both these quantities [13].

With a three phase voltage source inverter there are eight possible operating states. In (figure 4), the upper switch of the inverter's pole A is on whereas the lower switch is off. Contrary to this, on the other two legs, the upper switch is off while the lower switch is on for V (100) condition.

Because of the constraint that the input lines must at no time be shorted and the output current must always be continuous a voltage source inverter can assume only eight distinct topologies. Six out of these eight topologies yield a non-zero output voltage and are admitted as non-zero switching states and the remaining two topologies produce zero output voltage and are certified as zero switching states.

The space vector modulation (SVM) for three-leg VSI is positioned on the representation of the three phase quantities as vectors in a two-dimensional (□□□□ plane. This can be seen in the vector representation diagram. The voltages V_{ab}, V_{bc} and V_{ca} are three line voltage vectors displaced by 120 degrees in space.

The desired three phase voltages at the output of the inverter could be represented by an equivalent vector V_{ref}. The reference vector is then synthesized using combination of two adjacent active switching vectors and one or both of the zero vectors.

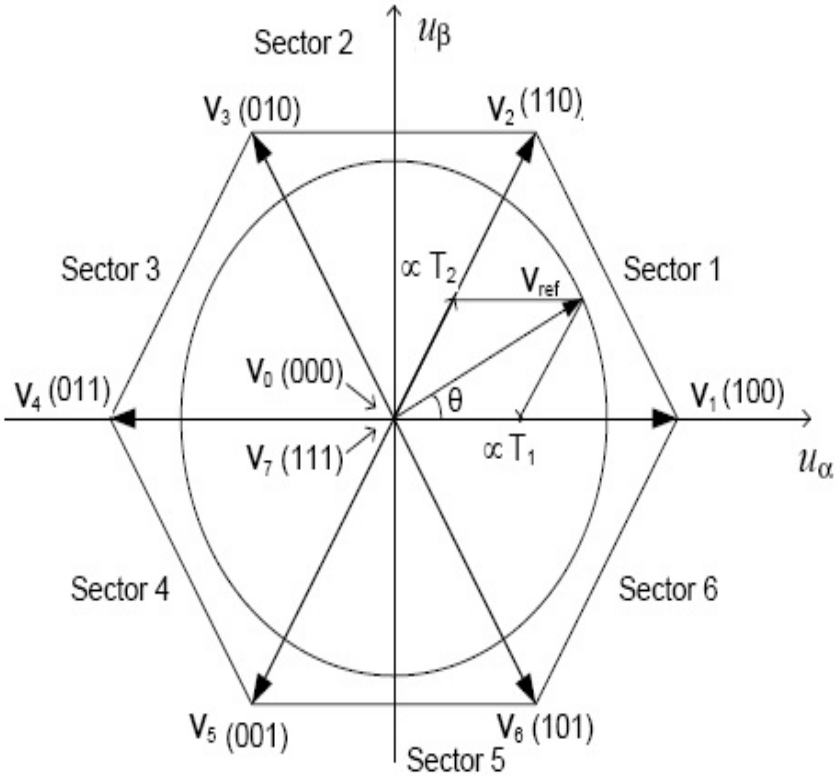

Figure 3. Vector Representation of SVM

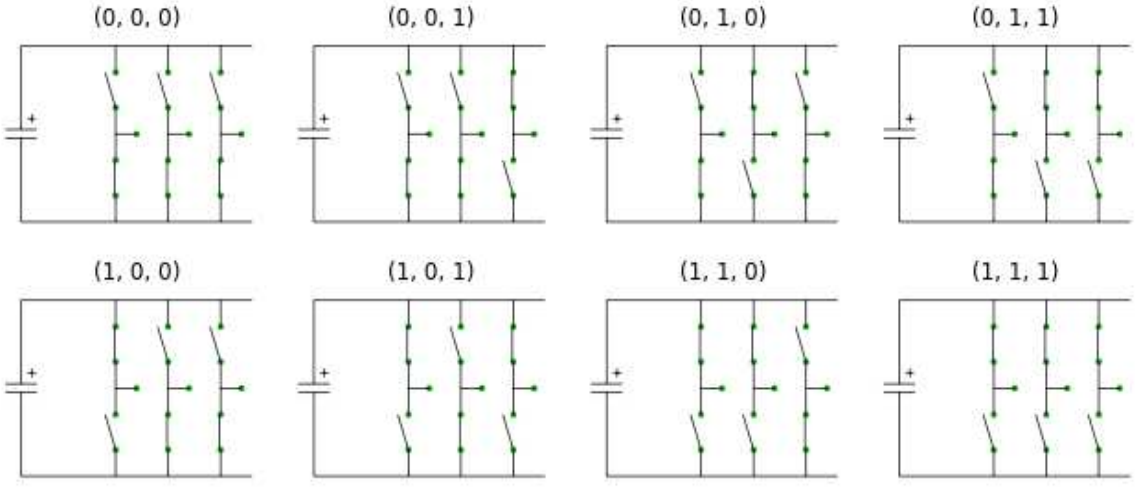

Figure 4. Eight Possible Switching States

Figure 3. Vector Representation of SVM

The magnitude
output voltage
revolution is the same as the principal time period of the output voltage.

. EXPERIMENTAL SETUP

The diagram below shows the circuit diagram of the proposed system. The input dc source of 90 V is used. A total of nine split source capacitors are used. The main function of split

source capacitor is to equally divide the input source to the switches. MOSFETs are used as the switches with the combination of diodes with it. A total of thirty two diodes are used. Also twelve MOSFET switches are used. A subsystem designated as "Out1" is used to provide the pulses to the gate of MOSFET and input to the triggering pulses block. The diodes are such connected that they are anti parallel to each other. Some of the MOSFET switches are individually used and the pulses are given through the subsystem interconnected to it. The voltage measurement and current measurement blocks are also used for ideal voltage and current measurement respectively. Series RL branch is also used to obtain the desired output. Finally the output is taken from the output voltage parameter.

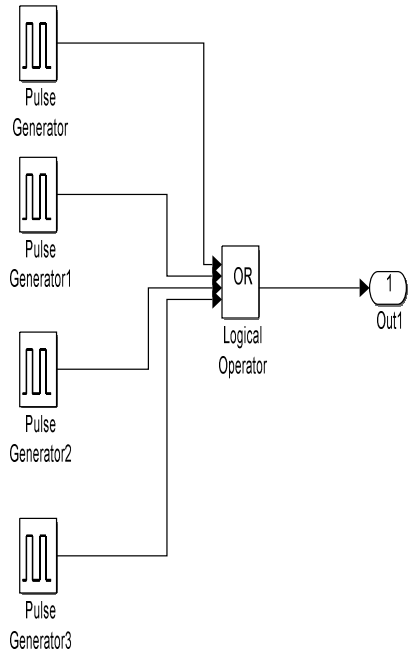

Figure 5. Subsystem of Generating Pulses

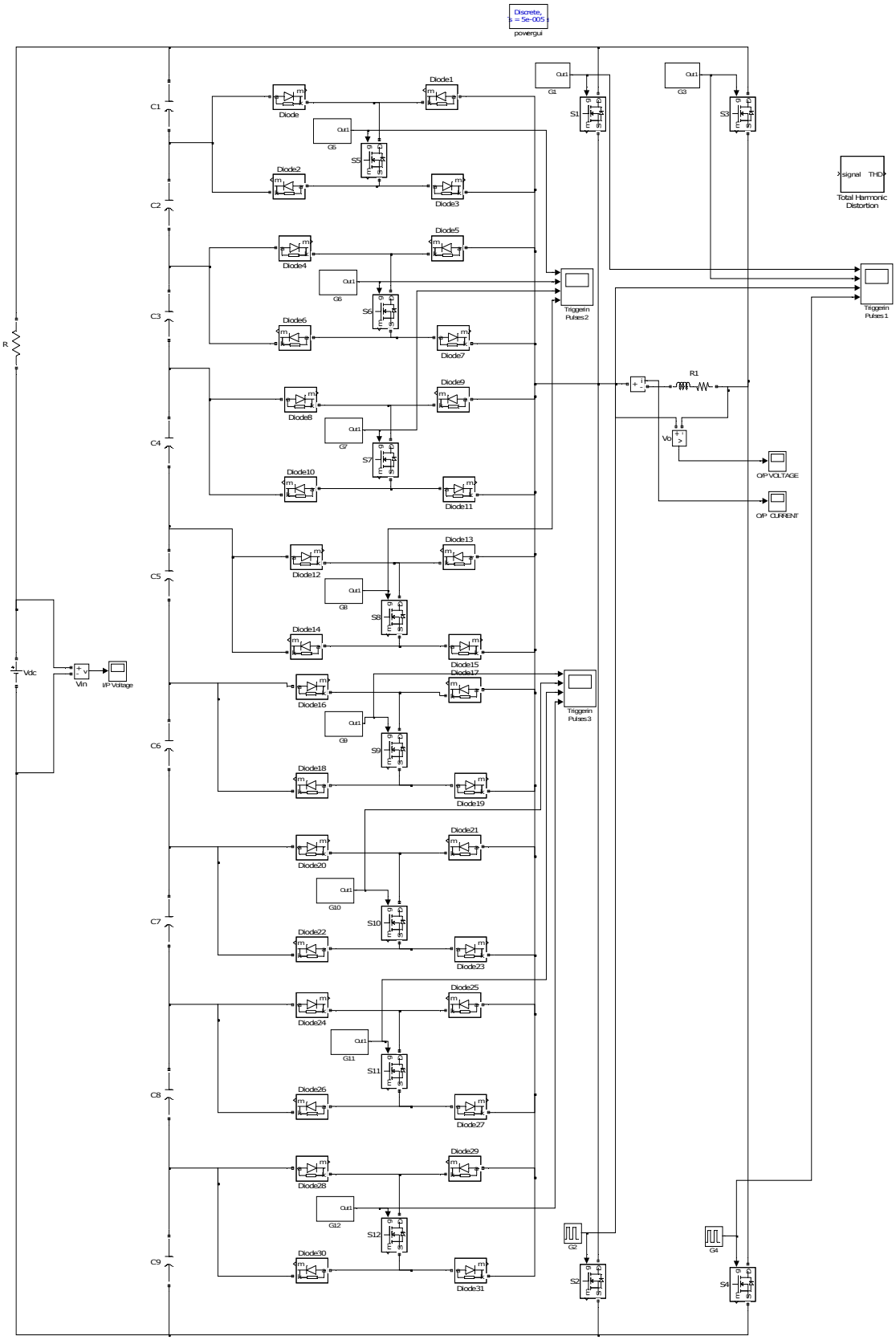

Figure 6. Circuit Diagram of Proposed System

5. SIMULATION RESULTS

This section deals with the simulation results of the proposed 19 level asymmetric multilevel converter. Single dc source of value 90V is used as the input source. The value of output voltage frequency is 50 Hz.

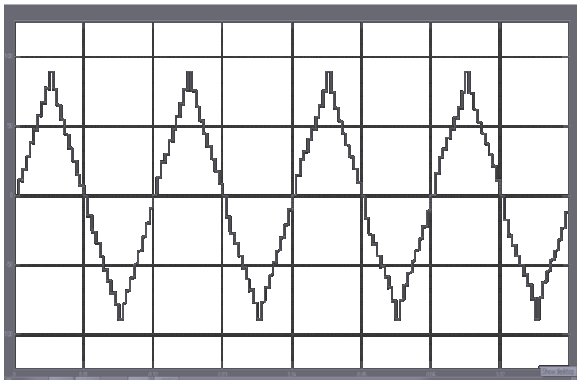

Figure 7. Output Voltage Waveform

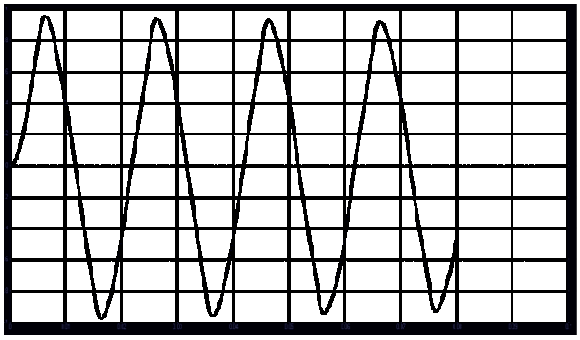

Figure 8. Output Current Waveform

The proposed system uses thirty two diodes with a combination of twelve MOSFETs as switches. For this case, the THD of the output voltage based on simulation is 5.70%. The efficiency of the converter is based on the applied control strategy. This paper uses fundamental frequency control strategy. Thus the efficiency of the converter is high.

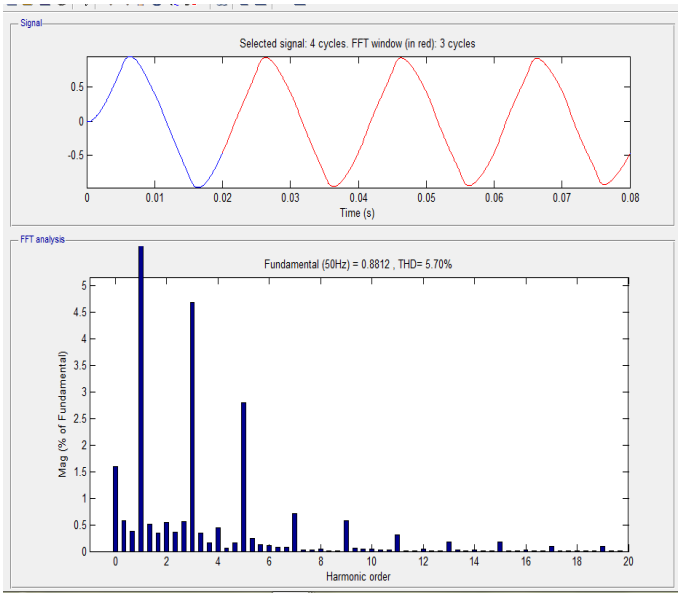

Figure 9. Harmonic Spectrum (THD 5.70%)

6. CONCLUSION

This paper proposes a new structure for asymmetric multilevel converter. This new structure minimizes the use of dc source and also increases the levels of output voltage waveform. This system is suitable for medium and high voltage applications. Because of the use of single dc source and less number of switches, the overall cost and complexity of the system is reduced. The fundamental frequency control strategy increases the efficiency of the converter.

7. FUTURE SCOPE

The proposed design can be further used to raise the level of output voltage. Also other power electronic components like IGBT can be used in place of MOSFET. The proposed structure can also be changed to get the desired number of levels which can also minimize the total harmonic distortion.

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